IN THE CLAIMS:

1. (Original) A method for performing a wire-bonding operation in an integrated circuit, comprising the following steps:

determining positions of at least one height-sensing pad and at least one bond pad on a top surface of an integrated circuit die, wherein the at least one height-sensing pad is electrically isolated from circuitry of the die and the at least one bond pad is electrically connected to the die circuitry;

lowering a bonding tool to the at least one height-sensing pad;

determining a height coordinate of the at least one height-sensing pad; and

wire-bonding the at least one bond pad to a lead of a leadframe utilizing the height coordinate of the at least one height-sensing pad.

2. (Original) The method of claim 1, further comprising the step of determining a height coordinate of the at least one bond pad.

3. (Original) The method of claim 2, wherein the height coordinate of the at least one height-sensing pad is used in determining the height coordinate of the at least one bond pad.

4. (Original) The method of claim 1, further comprising the step of adjusting ultrasonic power of the bonding tool after the height coordinate of the at least one height-sensing pad is determined.

5. (Original) The method of claim 1, wherein in the step of lowering a bonding tool comprises the step of lowering the bonding tool to a height-sensing pad adjacent to a starting bond pad, wherein the starting bond pad is the first bond pad, in a given set of bond pads of the die, to be bonded to a lead of the leadframe.

6. (Original) The method of claim 1, wherein the step of lowering a bonding tool comprises the step of lowering the bonding tool to a height-sensing pad adjacent to a terminating bond pad,

wherein the terminating bond pad is the last bond pad, in a given set of bond pads of the die, to be bonded to a lead of the leadframe.

7. (Original) The method of claim 1, wherein the at least one bond pad comprises a bond rail.

8. (Original) The method of claim 7, wherein the height-sensing pad is arranged adjacent to the bond rail.

9. (Original) The method of claim 1, wherein the at least one bond pad comprises a bond rail and a plurality of bond pads.

10. (Original) The method of claim 1, wherein the step of determining positions of at least one height-sensing pad and at least one bond pad comprises the step of scanning the top surface of the die.

11. (Original) The method of claim 10, wherein, in the step of scanning the top surface of the die, a surface/wire-feed detection system is used.

12. (Original) The method of claim 1, wherein the step of determining positions of at least one height-sensing pad and at least one bond pad comprises the step of manually programming the bonding tool with the positions of at least one height-sensing pad and at least one bond pad on the top surface of the die.

13. (Original) The method of claim 1, wherein the top surface of the integrated circuit die includes a plurality of height-sensing pads, each corresponding to one of a plurality of bond pads.

14. (Original) The method of claim 1, wherein the at least one height-sensing pad is disposed further from the die circuitry than the at least one bond pad.

15. (Original) The method of claim 1, wherein a height-sensing pad is disposed at each corner of the integrated circuit die.

16. (Original) The method of claim 1, wherein at least three height-sensing pads are disposed on the top surface of the integrated circuit die.

17. (Original) The method of claim 16, further comprising the step of determining a plane of the integrated circuit die from the height coordinates obtained from the at least three height-sensing pads.

18. (Original) The method of claim 17, further comprising the step of determining a tilt of the integrated circuit die with respect to the bonding tool using the plane of the integrated circuit die.

19. (Original) The method of claim 18, further comprising the step of determining the height coordinate of the at least one bond pad using the height coordinate of the at least one height-sensing pad and the tilt of the integrated circuit die.

20. (Canceled)